

Block diagram of a 270 kbps 8PSK transmitter. The input is a bit stream b_i (101) at 810 kbps. It passes through a "Serial to Parallel" block (108) to produce a 3-bit vector t_i (103). This vector is used to address an "8PSK ROM" (102) to produce a complex symbol a_i (105). The symbol a_i is multiplied by a carrier signal $e^{j3\pi/8}$ (104) in a multiplier block. The resulting signal is then passed through a "PAM" block (106) to produce the final output signal 110. The carrier signal is generated by a PLL block (107) which is locked to a 270 kbps reference signal.

FIG. 1A

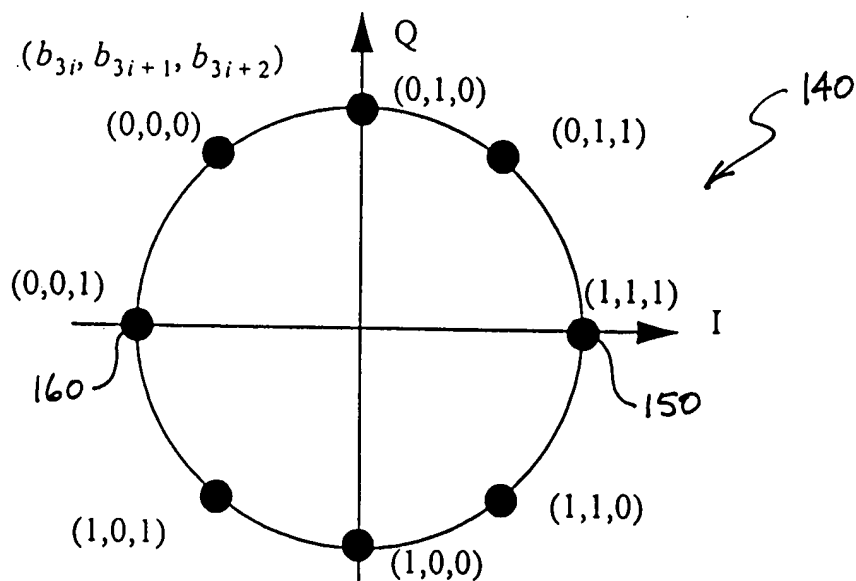


FIG. 1B

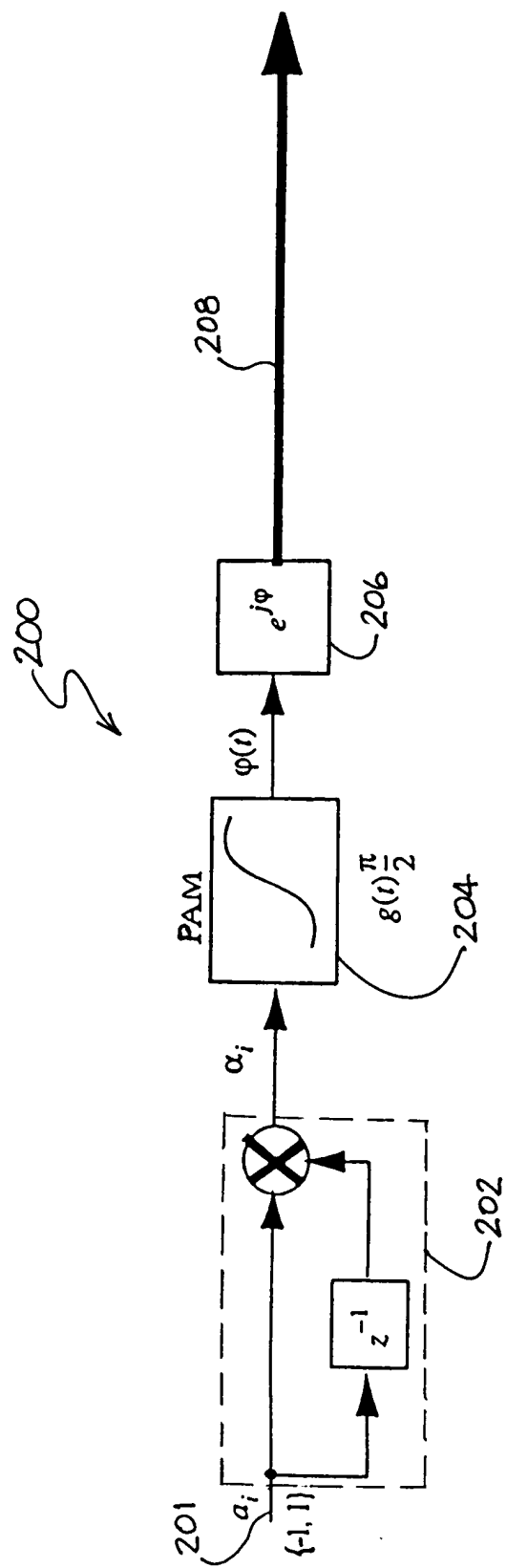


FIG. 2A

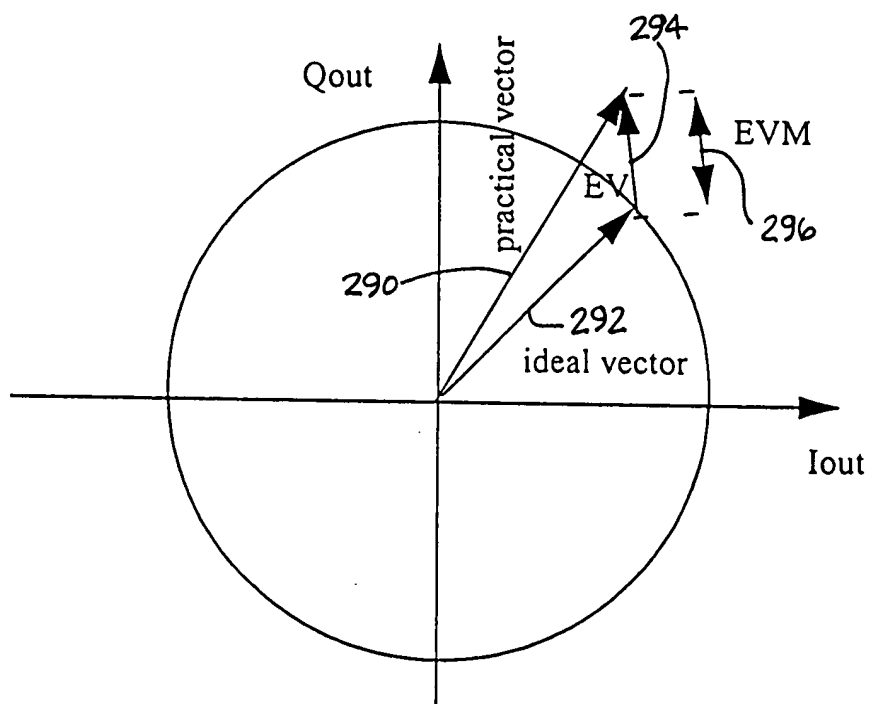


FIG. 2C

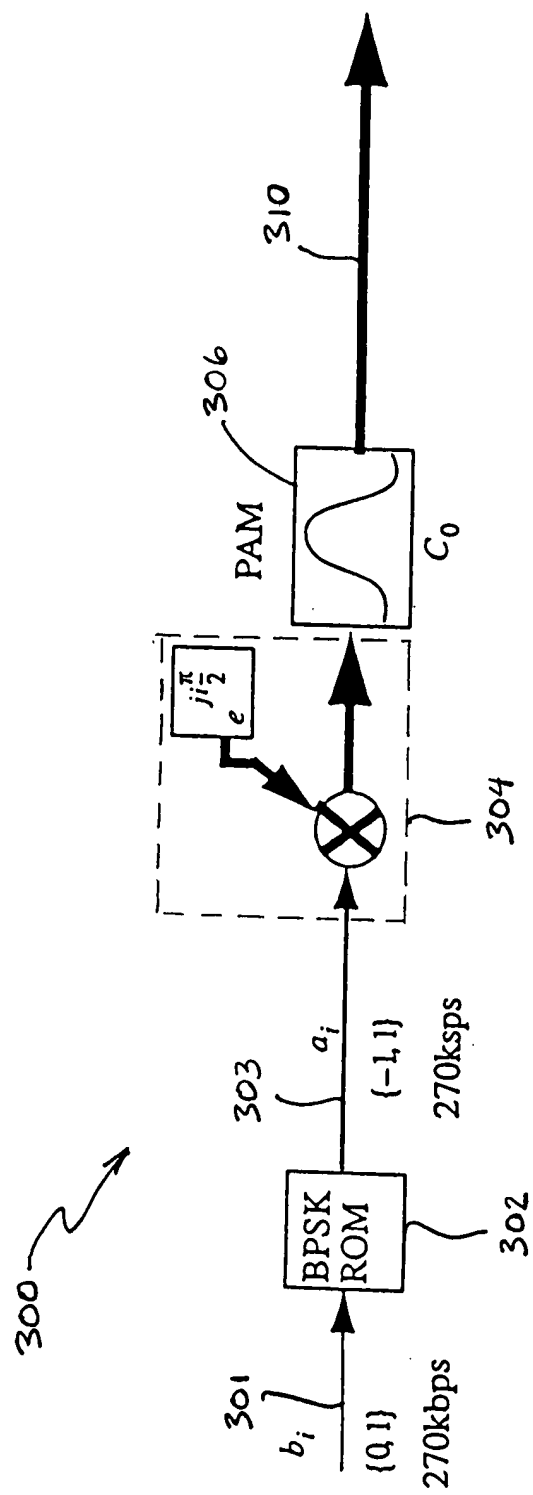


FIG. 3

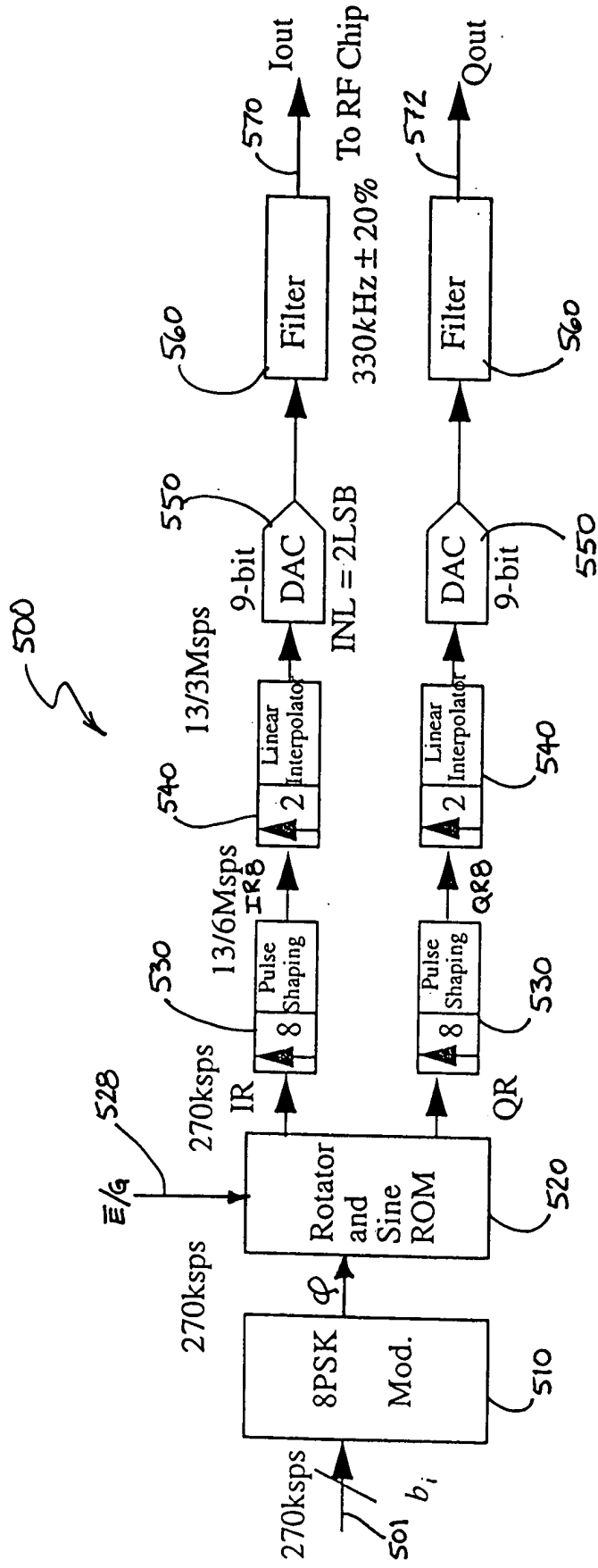


FIG. 5A

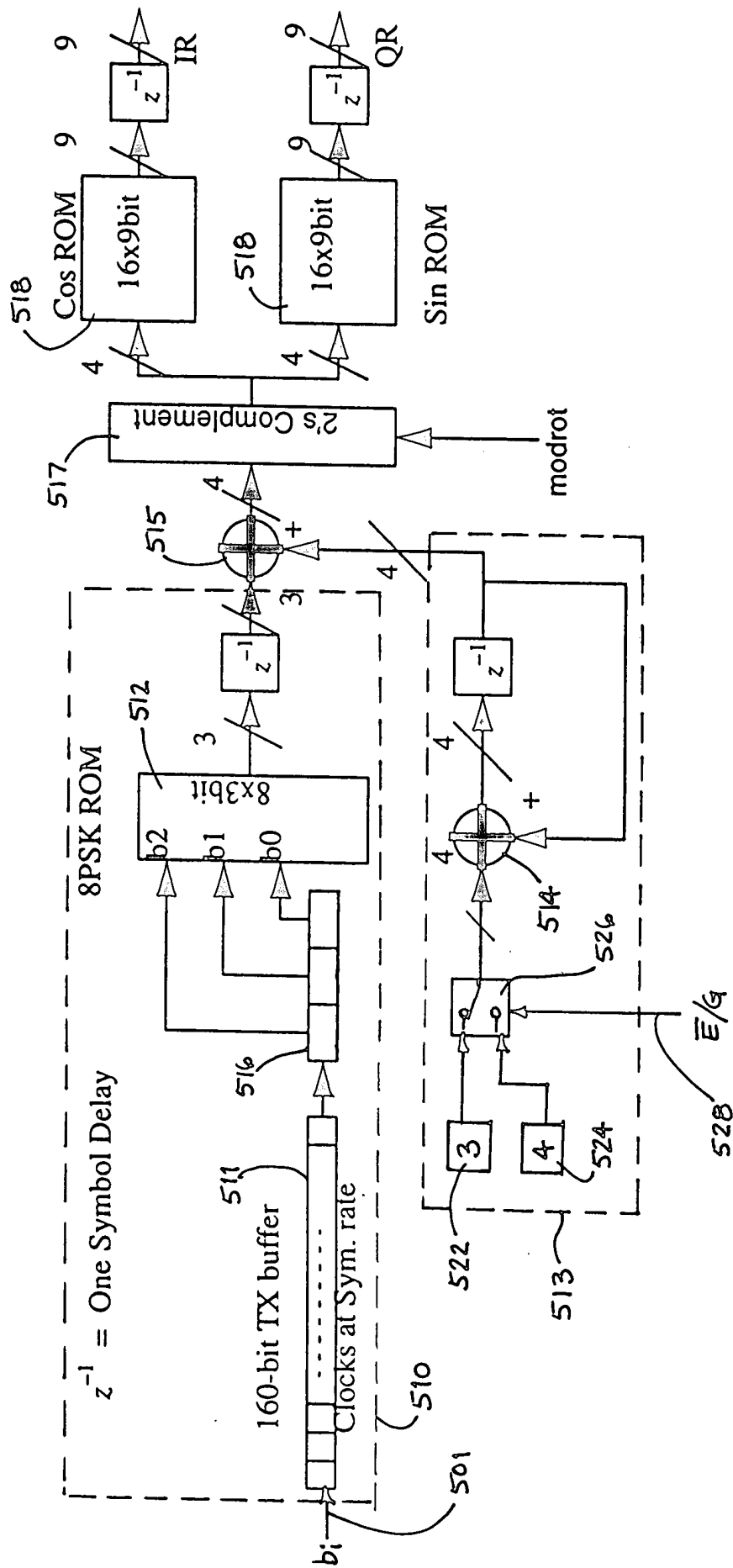


FIG. 5B

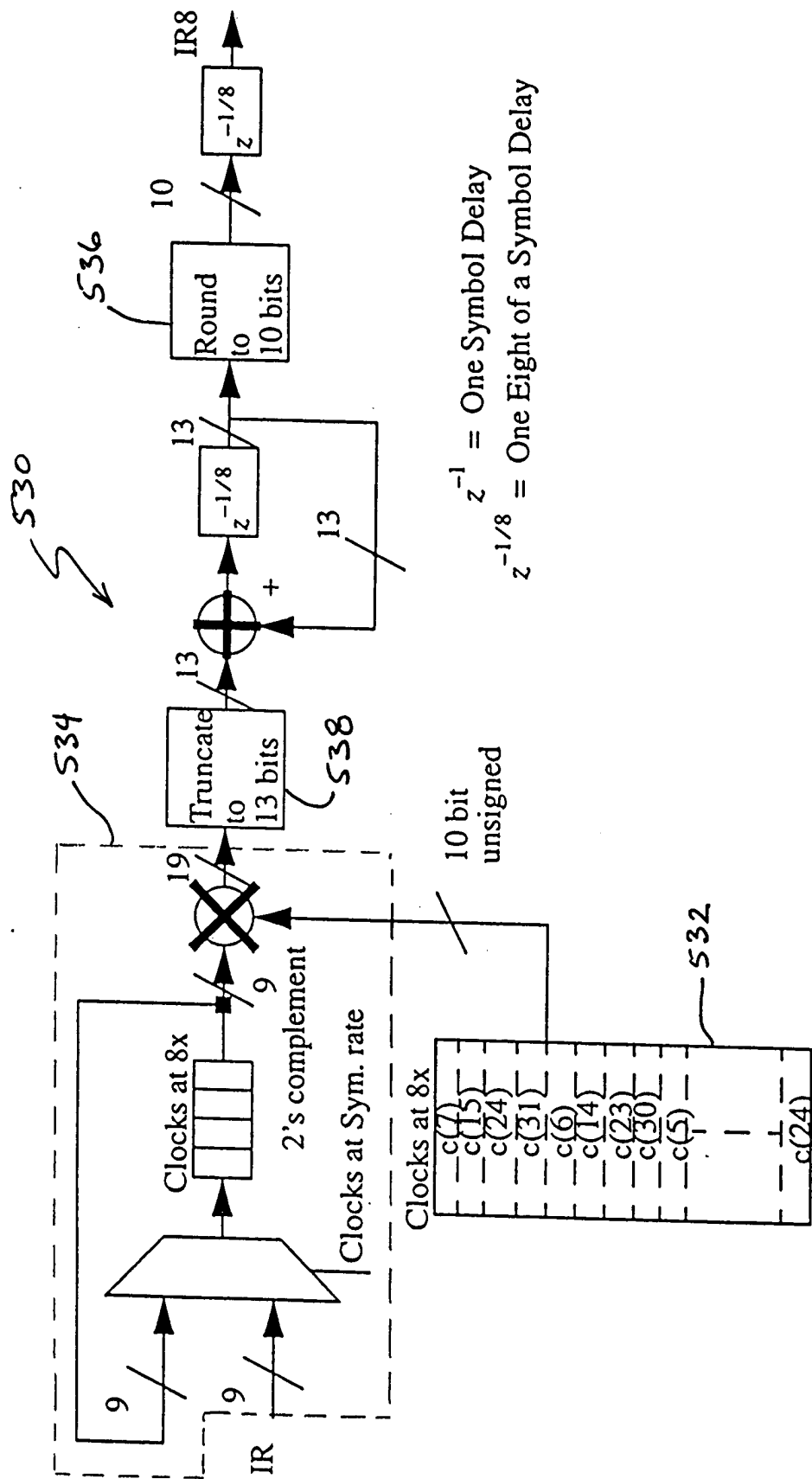


FIG. 5C

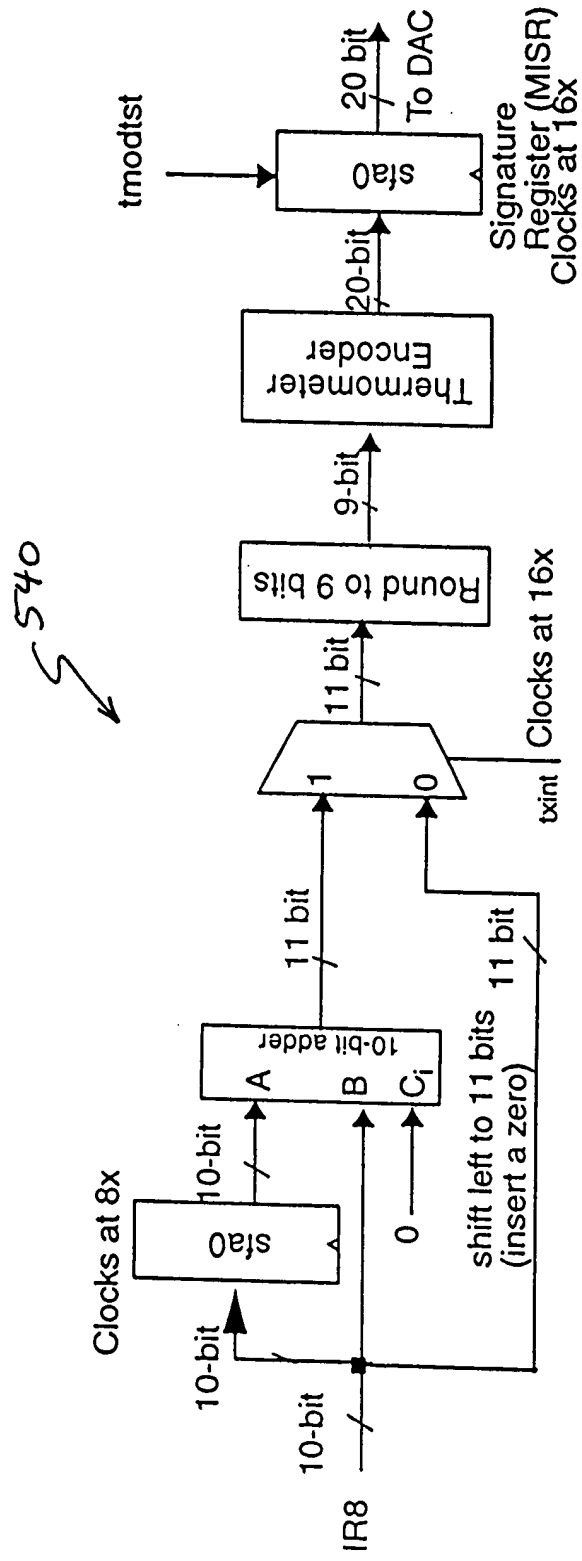


FIG. 5D

FIG. 6

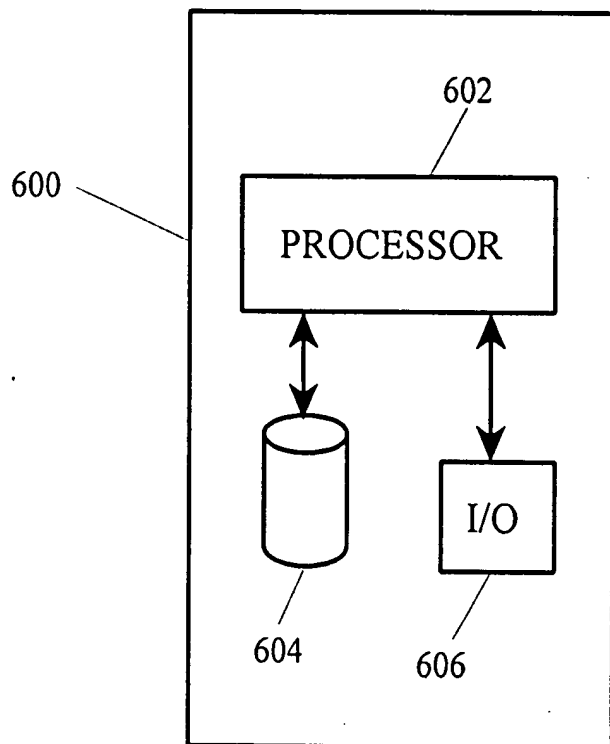


FIG. 6